INVESTIGATION OF CLOSED LOOP CURRENT CONTROL STRATEGIES FOR BRIDGELESS INTERLEAVED SEPIC CONVERTER

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Abstract. This paper presents current control strategies for a novel Bridgeless Interleaved SEPIC PFC Converter to regulate power factor correction. The strategies discussed in this paper are peak current control, Average current control and Non-Linear carrier control. Simulation work has been carried out in MATLAB/SIMULINK. The performance parameter of the converter is compared under open loop and closed loop conditions. Based on the results, the input current is observed to be close to sinusoidal implying a low harmonic profile and high power factor.

1 Introduction

Conventional switched mode power supplies comprise of a diode bridge rectifier with a filter capacitor. This draws highly distorted non-sinusoidal input current from the mains and thus they have harmonic rich distorted supply current. As per the norms of the international standards for power quality, it is recommended to have the power factor close to unity. To address this issue, power factor correction has become an integral part of switched mode power supplies. Active power factor correction circuits are adopted to maintain the power factor close to unity by controlling the current drawn by the load such that the supply current is proportional to the supply voltage so that a resistive behaviour is emulated. There are a number of power factor correction AC-DC converters available in the literature. However, SEPIC converter is one the popular topologies for active power factor correction as it can provide voltages higher or lower than the supply voltage and also a high power factor can be achieved. [1]

In this paper, various current control strategies such as Peak current, average current and Non-Linear carrier current control techniques for a novel Bridgeless Interleaved SEPIC Converter have been studied and analysed. These techniques have been simulated in MATLAB/Simulink. In section 2, the operation of Bridgeless Interleaved SEPIC PFC Converter is discussed. The working of the current control strategies is presented in section 3. Simulation results of the models are discussed in Section 4. A comparative analysis based on the performance parameters is carried out and the results show the effect of control strategies on the converter. The results are verified.

2 Bridgeless Interleaved SEPIC converter

Bridgeless Interleaved SEPIC Converter topology is shown in Fig.1. Construction wise, two more diodes and MOSFET switches are added to the input diode bridge rectifier. This topology exploits the benefits of bridgeless and interleaved topologies. As the Bridgeless topology eliminates the diode bridge, the heat management is resolved and thus conduction losses are
minimized. The interleaving topology divides the current stress in the semiconductor devices and the ripple in the supply current is also greatly minimized. [2]

![Bridgeless Interleaved SEPIC Converter](image)

With reference to Fig.1, when the supply voltage is positive, Q1/Q3 is switched on and current flows through L1-Q1-Q3-L3. During this period, energy is stored in L1 and L3. When Q1/Q3 is switched off, L1 and L3 releases its stored energy through C1 /C3, load and returns through the body diode of Q3 back to the input mains. The inductors connected to the Q1/Q3 leg on load side L5/L7 takes energy from the SEPIC capacitor C1 and C3 and the output capacitor supplies the load. During the negative half cycle, Q4/Q2 is turned on and current flows through L4 -Q4-Q2- L2, returning to the line; during this period, energy is stored in L4 and L2. When Q4/Q2 are turned off, L4 and L2 releases its stored energy and thus current flows through C2 /C4, load and returns through the body diode of Q2 back to the input mains. The inductors connected to the Q4/Q2 leg on load side takes energy from the SEPIC capacitor C2 and C4, and the output capacitor supplies the load. [3]

### 3 Current control strategies for Bridgeless Interleaved SEPIC Converter

The power factor obtained in the open loop configuration of the converter can be enhanced by adopting current control techniques. By introducing the feedback and feed forward loops, lower harmonic profile can be maintained[4]. The general control principle of the controller is that the supply current is forced to track a generated sinusoidal reference so that the converter draws a sinusoidal current; thereby power factor is improved. Generally two loops are implemented in the controller; to control the instantaneous input current to follow the same wave shape as the instantaneous input voltage, current feedback loop is implemented. The other loop is a voltage feedback loop which adjusts the input current so as to maintain a constant output voltage [5]. Many current control strategies have been reported in the literature. The following section highlights the implementation of peak current, average current and Non-Linear carrier control strategies for Bridgeless Interleaved SEPIC Converter. To operate the converter as a power factor corrector, we consider continuous conduction mode as the current stress and current ripple are minimum in this mode.
3.1 Peak Current control

Fig. 2. Peak Current control of Bridgeless Interleaved SEPIC Converter

The working of peak current mode control (refer Fig.2) is as follows. In the outer voltage loop, $V_{\text{error}}$ is generated by comparing the output voltage of the converter with a reference voltage. The voltage error and the input sinusoidal reference current are multiplied to generate a reference current in such a way such that it traces the peak of the inductor current. The upslope of inductor current is compared with this reference current. Whenever the inductor current crosses zero, switch is turned on and as it reaches the reference current, the flip-flop is reset and the switch is turned off. [5-8]

3.2 Average Current Control

This technique allows a better input current waveform than the peak current control method as a Current error amplifier (CEA) is introduced in this technique. Average Current control technique (refer Fig.3) is a two loop control method; it has as an inner current control loop and an outer voltage control loop. This CEA output which is the difference between the average inductor current and the voltage error provided by the outer loop is then compared with a large amplitude ramp waveform with the converter switching frequency using Pulse Width Modulation (PWM) comparator. Thus, the average of inductor current is taken as the reference and the inductor current is forced to follow it. The switch is turned on whenever the inductor current reaches zero and switch is turned off when the inductor current falls below the reference. The voltage Error Amplifier forces the converter output voltage to track the voltage reference by controlling the average inductor current. [5-9].
3.3 Non-Linear Carrier Control

In this technique, a negative ramp carrier waveform is generated. There are two ways of controlling the duty cycle through this method. One is by inductor current sensing and the other method is switch current sensing. The controller generates the pulses from the comparison of the negative ramp carrier waveform and the sensed inductor current signal as shown in Fig 4a or sensed switch current signal as shown in Fig 4b.
The sinusoidal switch current/Inductor current is sensed to compare with the nonlinear carrier waveform in each switching period to achieve the sinusoidal input current wave shape or high power factor condition. The distinguishing feature of this technique is that it eliminates multiplier, voltage sensor and current error amplifier circuits in the controller loop [9-10]. Thus this controller offers improved performance over the other schemes.

4 Simulation Results

The simulation results of the current control strategies for Bridgeless Interleaved SEPIC converter are discussed in this section. In this work, the converter is designed with the simulation parameters as follows; \( V_{in} = 24\)V, 50Hz, \( V_o = 48\)V, \( f_{sw} = 25\) KHz Duty Cycle=59%, \( L_1 \ L_2 \ L_3 \ L_4 = 2.8\)mH, \( L_5 \ L_6 \ L_7 \ L_8 = 4.03\)mH, \( C_1 \ C_2 \ C_3 \ C_4 = 6.7\)µF and \( C_p = 3200\)µF. The performance of the converter is analyzed by computing parameters such as Total Harmonic Distortion (THD), Distortion factor \( K_d \), Displacement factor \( K_\theta \) and power factor.

The simulation results of the peak current control mode are shown in Fig.5. It is found that the THD in this mode is 5.38%. Thus the power factor is higher than the open loop configuration of the converter.

![Fig.5. Simulation results of Peak current control of Bridgeless Interleaved SEPIC converter.](image)

The simulation results of the average current control mode are shown in Fig.6. From Fig.6b, it is observed that the THD is 4.20% and is lower than the peak current control.

![Fig.6. Simulation results of Average current control of Bridgeless Interleaved SEPIC converter.](image)
Fig. 6. Simulation results of Average current controlled Bridgeless Interleaved SEPIC Converter. (a) Supply voltage and supply current (b) Output voltage (c) FFT Analysis of supply current

Fig.7 and Fig.8 shows the simulated results of the non-linear current mode by inductor current sensing and switch current sensing respectively. It is observed that the THD is very much improved than the previously discussed control techniques.
Table.1 shows the comparison between the performance parameters of open loop and closed loop configuration of Bridgeless Interleaved SEPIC Converter.

<table>
<thead>
<tr>
<th>Bridgeless Interleaved SEPIC Converter Topology</th>
<th>THD (%)</th>
<th>$K_d$</th>
<th>$K_θ$</th>
<th>Power Factor</th>
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<tr>
<td>Open Loop</td>
<td>6.26</td>
<td>0.9980</td>
<td>0.9903</td>
<td>0.9883</td>
</tr>
<tr>
<td>Peak Current</td>
<td>5.38</td>
<td>0.9986</td>
<td>0.9944</td>
<td>0.9929</td>
</tr>
<tr>
<td>Average Current</td>
<td>4.20</td>
<td>0.9991</td>
<td>0.9945</td>
<td>0.9936</td>
</tr>
<tr>
<td>Non-Linear carrier Current, Inductor current sensing</td>
<td>3.90</td>
<td>0.9992</td>
<td>0.9956</td>
<td>0.9950</td>
</tr>
<tr>
<td>Non-Linear carrier Current, Switch current sensing</td>
<td>3.42</td>
<td>0.9994</td>
<td>0.9963</td>
<td>0.9955</td>
</tr>
</tbody>
</table>

From Table 1, it is evident that the closed loop strategies enhance the power quality. Among the current control strategies, we find that the Non-Linear carrier control has power factor close to unity and thus considered more effective.

5 Conclusion

In this paper, a novel Bridgeless Interleaved SEPIC Converter for power factor correction has been discussed and it is found that it has a better harmonic profile compared to other active PFC topologies. To improve the supply current quality, the current control techniques like peak current, average current and Non-Linear carrier control techniques have been incorporated. The validity of the designed control strategies have been verified by MATLAB simulation. Simulation results shows that the closed loop strategies significantly increase the power quality and the supply current follows the supply voltage very closely. From the results, it is obvious that the Non-Linear carrier control has lower THD and high power factor and thus proves to be more suitable control strategy for power factor correction.

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REFERENCES


