PERFORMANCE OF MOS CAPACITORS WITH SI AND GAAS SUBSTRATES, LA_2O_3 AS GATE OXIDE

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ABSTRACT

The continual dimensional scaling of MOS devices requires a recurrent search for new materials for enhanced device performance. Hence, we present a work on simulation of two nano MOS capacitors – one using the dimensionally scaled conventional materials viz., Si substrate, La_2O_3 oxide layer and Al as gate contact conductor material and the other nano MOS capacitor using GaAs substrate, La_2O_3oxide layer, Al gate contact. Both the MOS devices are simulated for determining Charge density, Electric field, Device potential and Energy with respect to Distance (in nm). The mentioned parameters are compared for both the nano MOS devices for further analysis.

KEYWORDS

GaAs, MOS Capacitor, Charge Density, Potential, Energy, Substrate material, Lanthanum Oxide.

1. INTRODUCTION

During the recent days, Silicon substrate is not showing a better performance and efficiency in microwave Integrated Circuits (IC). So, an alternate to silicon substrate has been chosen to be Gallium arsenide (GaAs) due to its higher saturated electron velocity and higher electron mobility which allows the ICs to function at frequencies above 250GHz. At higher frequencies, every electronic system normally designed with Si substrate dissipates more power and heat. But the systems or devices which use GaAs as their substrate are relatively very insensitive to overheating due to their wider energy band gap and are less noisy than the systems or devices which use Si substrate. So, as a result electronic circuits to operate at high frequencies require GaAs as its substrate to cater the needs of applications in satellite communications, microwave point to point links and higher frequency radar systems which normally have to operate at very high frequencies. The major advantage constrained to GaAs is its speed since the electrons travel five times faster in GaAs than they do in Si. So GaAs is faster than Si and is more suitable for electronic systems like mobile phones and high speed computers [1].

The conventional Metal-Oxide-Semiconductor (MOS) structure is obtained by growing a layer of SiO_2 on top of silicon substrate and then depositing a layer of poly-silicon for gate metal contact [2]. Traditional silicon MOS device scaling has driven the semiconductor industry for the past four decades and in recent years, new materials and processes have been introduced to maintain pace with Moore's law which states the development of high density integrated circuits. Aiming at higher device performances like low power consumption and high frequency operations, the MOS devices dimensions are going down from submicron to nano meter scales [3-4].

However, the drastic reduction in the dimensions will not always support the enhancement in device performance and this is the main reason to estimate the performance of the MOS

capacitors with Si and GaAs substrates with La_2O_3 as their gate oxide material through energy band diagrams by considering parameters like charge density (ρ), electric field (E), potential (V) and energy (eV) [5-8].

The organization of the paper is as follows. Section 2 describes the proposed MOS capacitors. Section 3 presents the results and discussion. Section 4 concludes the paper.

2. PROPOSED MOS CAPACITORS

The nano MOS capacitors are built layer by layer using simulation software developed by Richard G. Soutwick et.al of Boise State University which has inbuilt database of substrates, oxide layers and gate metal contact materials. For the first nano N-MOS capacitor, conventional materials i.e., Silicon (Si) of 50nm thickness as substrate, Lanthanum Oxide (La_2O_3) of 2nm thickness as oxide layer and Aluminium of 2nm thickness as gate contact material are selected.
For the other N-MOS capacitor, conventional material Si has been replaced with GaAs of 50nm thickness as substrate, Lanthanum Oxide (La_2O_3) of 2nm thickness as oxide layer and Aluminium of 2nm thickness as gate contact material are selected. The structures of Si substrate and GaAs substrate MOS capacitors with La_2O_3 as gate oxide are shown in figures Fig. 1 and Fig. 2 respectively. The properties of the materials used are tabulated in Table 1.

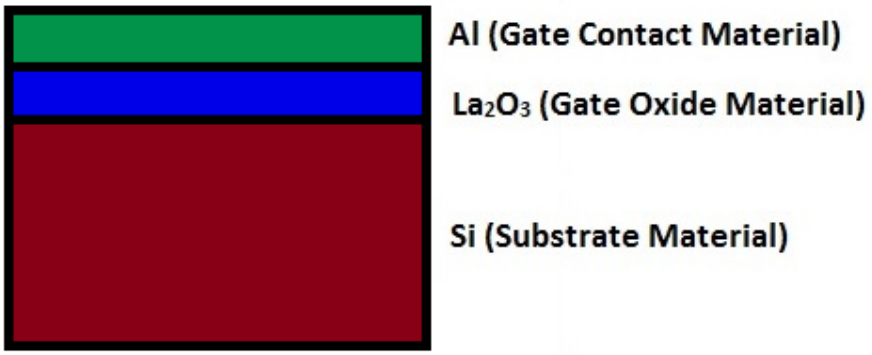

Fig. 1 Structure of MOS capacitor with Silicon substrate and La2O3 gate oxide

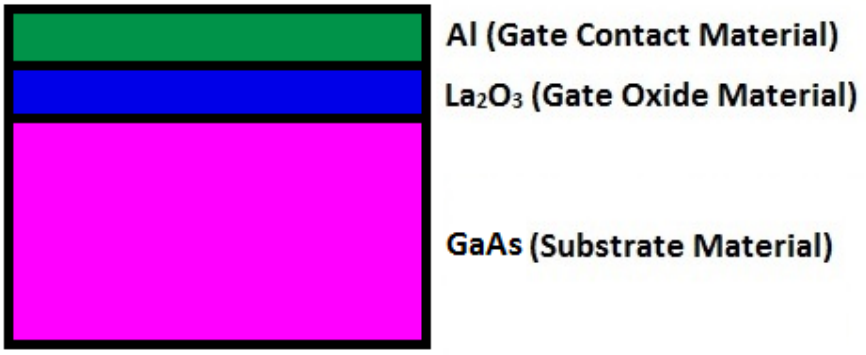

Fig. 2 Structure of MOS capacitor with GaAs substrate and La2O3 gate oxide

Table 1 Properties of materials used for MOS Capacitors with Si and GaAs substrates

Gate Contact Material	**Aluminium**	
Work Function	4.2	
Thickness	2nm	
Gate Oxide Material	**La_2O_3**	
Band Gap (eV)	6	
Dielectric Constant	25	
Electron Affinity(eV)	1.85	
Thickness (nm)	2	
Substrate Material	**Si**	**GaAs**
Dopant Concentration (atoms/cm^3)	10^{18}	10^{19}
Dielectric constant	11.7	13.1
Electron Affinity (eV)	4.05	4.07
Band Gap (eV)	1.125	1.42
Intrinsic Carrier Concentration (cm^{-3})	$1.42*10^{10}$	$0.09*10^{10}$

3. RESULTS AND DISCUSSION

Performance parameters like charge density (ρ), electric field (E), potential (V) and energy (eV) of the proposed MOS capacitors are studied using band diagram analysis. Both the devices are simulated with the gate voltage of -2.0 to +2.0V range at 300K temperature.

3.1. Charge Density

The charge density of MOS capacitor with Si Substrate and La_2O_3 gate oxide material is shown in Fig. 3. In Fig. 3, the dark green line represents the charge density of Aluminium (Al) gate contact, blue line represents the charge density of La2O3 oxide material and the brown line represents the charge density of Si substrate. For the applied gate voltage of +2V, MOS capacitor with Si substrate shows the charge density of 0.000018C/cm^2 for Al, 0C/cm^2 for La_2O_3 (since dielectric is an insulator) and -0.000064C/cm^2 for Si substrate and then reached zero at and after 0.2nm transition distance approximately.

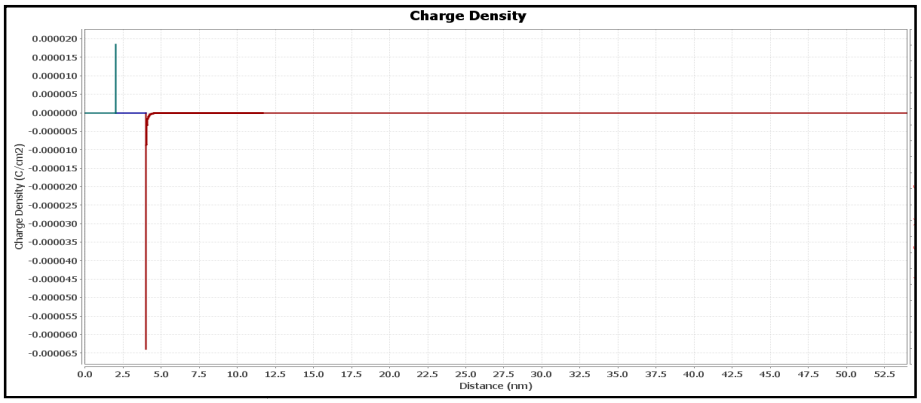

Fig. 3 The charge density of the Si substrate MOS capacitor

The charge density of MOS capacitor with GaAs Substrate and La_2O_3 gate oxide material is shown in Fig. 4. In Fig. 4, the dark green line represents the charge density of Aluminium (Al) gate contact, blue line represents the charge density of La_2O_3 oxide material and the pink line represents the charge density of GaAs substrate. For the applied gate voltage of +2V, the MOS capacitor with GaAs substrate shows the charge density of 0.000018C/cm^2 for Al, 0C/cm^2 for La_2O_3 (since dielectric is an insulator) and -0.000058C/cm^2 for GaAs substrate and then reached zero at and after 0.2nm transition distance approximately.

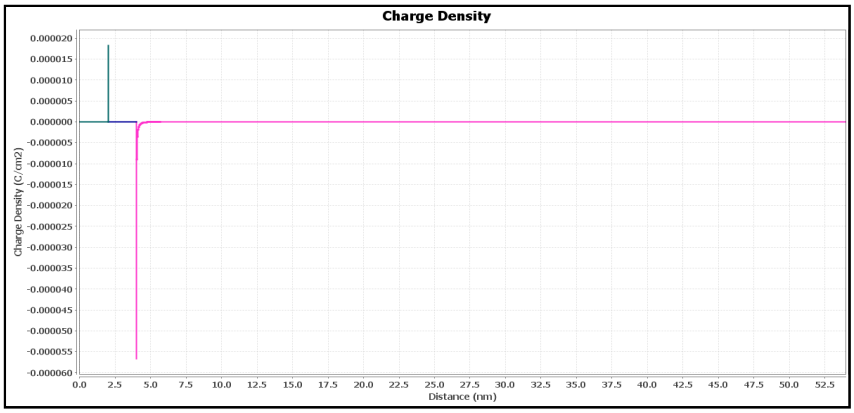

Fig. 4 The charge density of the GaAs substrate MOS capacitor

3.2. Electric Field

The Electric Field of the MOS capacitor with Si substrate is shown in Fig. 5. In the Fig. 5, the dark green line represents the electric field of Al, blue line represents the electric field in La_2O_3 and the brown line represents the electric field in Si substrate. For the applied gate voltage of +2V, the graph shows the rise of electric field till 8.7MV/cm and the same field is maintained in La_2O_3 up to 2.5nm transition distance approximately. Then a sudden rise of electric field in Si substrate is observed at 5nm distance approximately and then reached zero.

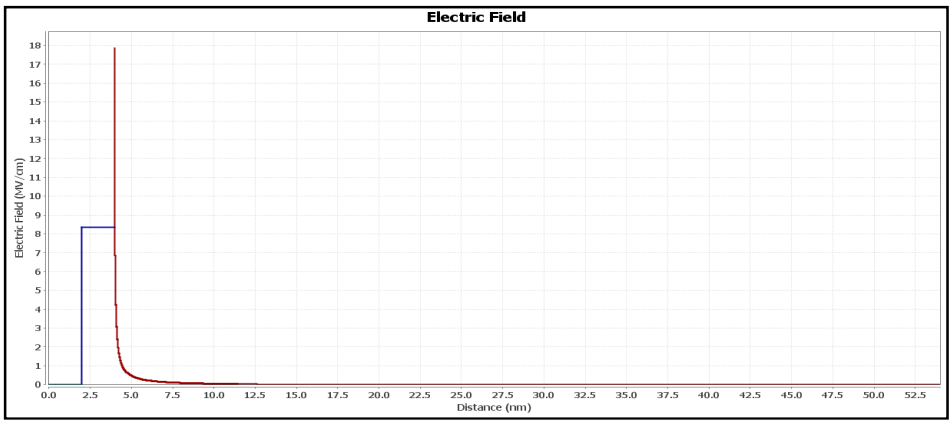

Fig. 5 The Electric Field of the Si substrate MOS capacitor

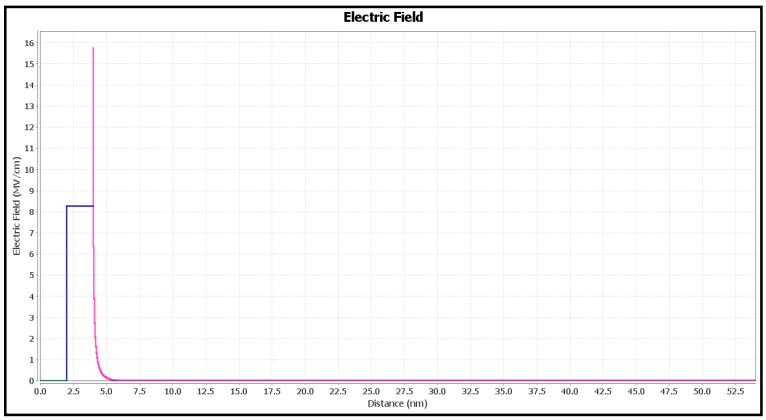

Fig. 6 The Electric Field of the GaAs substrate MOS capacitor

The Electric Field of the MOS capacitor with GaAs substrate is shown in Fig. 6. In the Fig. 6, the dark green line represents the electric field of Al, blue line represents the electric field in La_2O_3 and the pink line represents the electric field in GaAs substrate. For the applied gate voltage of +2V, the graph shows the rise of electric field till 8.7MV/cm and the same field is maintained in La_2O_3 up to 2.5nm transition distance approximately. Then a sudden rise of electric field in GaAs substrate is observed at 5nm distance approximately and then reached zero.

3.3. Energy

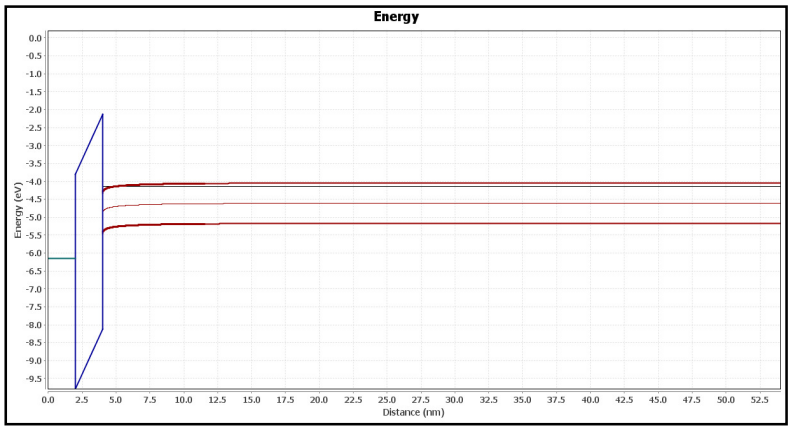

Fig. 7 The Energy of the Si substrate MOS capacitor

The Energy of the MOS capacitor with Si substrate is shown in Fig. 7. In the Fig. 7, the dark green line represents the energy band of Al, blue polygon region represents the energy band of La_2O_3 and the brown line represents the energy band of the Si substrate. The Al material has the energy of -6.1eV till the distance of 2.5nm approximately and the energy band bending can be observed in La_2O_3 due to the applied gate bias voltage. As the positive voltage is applied, the energy band shifts downward and allows the electrons to flow towards the other side (towards the oxide layer) if the empty bands are present below the Fermi level. From the Fig. 7 it can be inferred that there is a possibility for the electrons to tunnel towards the La_2O_3 layer as less energy of L2 i.e., -6.1eV has been observed compared to that of Si substrate which is -4.7eV approximately. The height of tunnelling barrier is 10.8eV which is observed from the energy band gap between the Si substrate and La_2O_3 oxide layer.

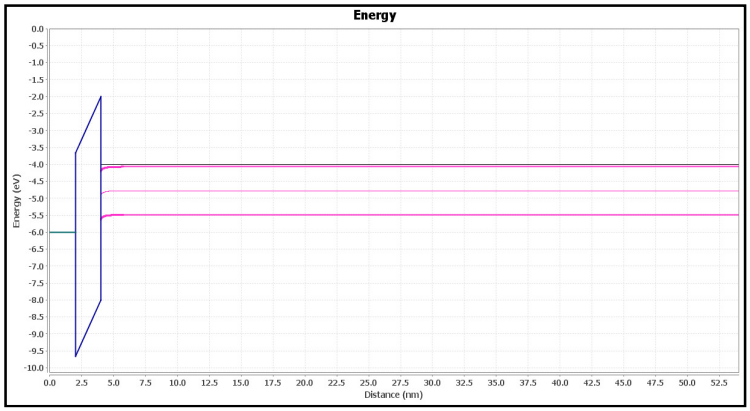

Fig. 8 The Energy of the GaAs substrate MOS capacitor

The Energy of the MOS capacitor with GaAs substrate is shown in Fig. 8. In the Fig. 8, the dark green line represents the energy band of Al, blue polygon region represent energy band of La_2O_3 and the brown line represents the energy bands of GaAs substrate. GaAs has the energy of -6.1eV and band bending can be observed in La_2O_3 material. From Fig. 8, it can be inferred that there is possibility of electrons to tunnel from GaAs substrate to Al contact through the oxide layer. The height of the tunnelling barrier is 7.6eV which is lesser compared to that of La_2O_3. So, the transition probability of tunnelling is lower in GaAs MOS capacitor because of the higher barrier height and less barrier width.

3.4. Potential

The Potential of the MOS capacitors with Si and GaAs substrates are shown in Fig. 9 and Fig. 10 respectively. From Fig. 9 and Fig. 10, it can be inferred that there is no much difference in the potential of the MOS capacitor with Si and GaAs substrates and hence the channel conductance and the ability of the oxide material to shield the electric field depends on the applied drain voltage.

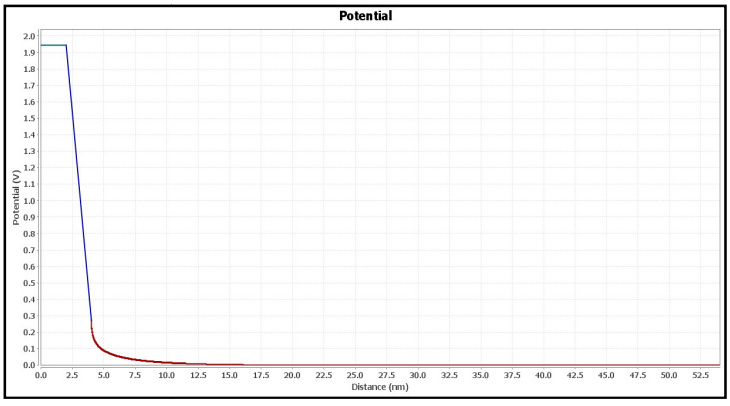

Fig. 9 The Potential of the Si substrate MOS capacitor

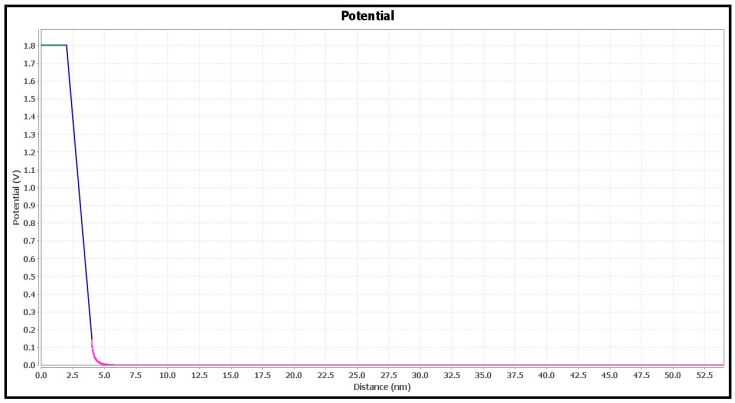

Fig. 10 The Potential of the GaAs substrate MOS capacitor

The parameters of the MOS capacitors with Si substrate to measure the performance are compared against the parameters of the of the MOS capacitor with GaAs substrate and are shown in Table 2. From Table 2 it can be inferred that MOS capacitor with GaAs substrate has lower threshold voltage and can be considered to be faster compared with the MOS capacitor with Si substrate.

The flat band voltage of MOS capacitor with GaAs substrate is higher that the flat band voltage of the MOS capacitor with Si substrate which signifies the stability since there is no electrical charge in the semiconductor which in turn infers that there is no voltage drop across it.

Table 2 Parameters of MOS capacitors with Si and GaAs substrates

Parameter	**MOS capacitor with Si Substrate**	**MOS capacitor with GaAs Substrate**
Flat Band Voltage (V)	0.055	0.197
Equivalent Oxide Thickness (nm)	0.312	0.312
Total Capacitance (μ F/cm^2)	10.74	10.74
Threshold Voltage (V)	-0.930	-2.043

4. CONCLUSION

Two n-type nano MOS capacitors are modelled using the software developed by Boise State University – one with Si substrate, La_2O_3 oxide layer, Al gate contact and the other with GaAs substrate, La_2O_3 oxide layer and Al gate contact. Both the MOS devices are simulated for charge density, electric field, energy and potential. Respective graphs are compared. From the comparison it is known that the MOS capacitor with GaAs substrate drives high drain current compared to the MOS capacitor with Si substrate which proves the suitability of it to the ICs which operate at microwave frequencies and faster applications.